AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0016] with the following replacement paragraph [0016]:

[0016] Figure 3 is a block diagram of an FPGA test circuit of an embodiment of the present invention; ~~and~~

Please replace paragraph [0017] with the following replacement paragraph [0017]:

[0017] Figure 4 illustrates an FPGA coupled to a tester circuit; and

Please add the following paragraph directly after paragraph [0017]:

[0017.1] Figure 5 is a flow chart of the method of testing a serializer/deserializer (SERDES) circuit of a field programmable gate array (FPGA).

Please add the following paragraph directly after paragraph [0028]:

[0028.1] Figure 5 is a flow chart of the method of testing a serializer/deserializer (SERDES) circuit of a field programmable gate array (FPGA).